WHAT IS CLAIMED:

1. A semiconductor die stack comprising:

a. at least two semiconductor dies vertically stacked upon each other, each semiconductor die defines opposed top and bottom surfaces and opposed pairs of longitudinal and lateral side surfaces; and

b. leads which extend out from at least one of the side surfaces of each of the semiconductor dies, the leads define first end portions, middle portions, second end portions, first junctions and second junctions, the second junctions of the leads of the upper semiconductor die are electrically connected to respective ones of the first junctions of the leads of the lower semiconductor die, the first and second junctions of the leads of the upper and lower semiconductor dies are bent in opposing directions.

2. The semiconductor die stack of Claim 1 wherein the middle portions of the leads of the upper semiconductor die are electrically connected to respective ones of the first junctions of the leads of the lower semiconductor die.

3. The semiconductor die stack of Claim 2 wherein a bend radii, bend distances and bend angles of the first junctions of the leads of the upper and lower semiconductor dies are equal to each other.

4. The semiconductor die stack of Claim 3 wherein the second junctions of the leads of the upper semiconductor die have a flared ski tip configuration.

5. The semiconductor die stack of Claim 1 wherein the first junctions of the leads of the upper semiconductor die are electrically connected to respective ones of the middle portions of the leads of the lower semiconductor die.

6. The semiconductor die stack of Claim 5 wherein bend distances of the first junctions of the leads of the upper semiconductor die are greater than the bend distances of the first junctions of the leads of the lower semiconductor die.

7. The semiconductor die stack of Claim 6 wherein the difference between the bend distances of the first junctions of the leads of the upper and lower semiconductor dies is at least a width of the leads of the lower semiconductor die.

8. The semiconductor die stack of Claim 7 wherein the second junctions of the leads of the upper semiconductor die have a flared ski tip configuration.

9. The semiconductor die stack of Claim 1 wherein the middle portions of the leads of the upper semiconductor die are electrically connected to respective ones of the middle portions of the leads of the lower semiconductor die.

10. The semiconductor die stack of Claim 1 further comprising at least one narrow jumper strip electrically connected to adjacent leads of at least one of the semiconductor dies.

11. The semiconductor die stack of Claim 10 wherein the narrow jumper strip(s) is electrically connected to the middle portions of the adjacent leads.

12. The semiconductor die stack of Claim 11 wherein the narrow jumper strip has a cross sectional area along its length equal to a cross sectional area along the height of the leads to which the narrow jumper strips are attached.

13. The semiconductor die stack of Claim 12 wherein the narrow jumper strip(s) may be fabricated from the same material as the leads of the semiconductor die.

14. The semiconductor die stack of Claim 1 further comprising at least one wide jumper strip electrically connected to at least two leads of at least one of the semiconductor dies, the at least two leads which are electrically connected to the wide jumper strip have at least one interposed lead therebetween.

15. The semiconductor die stack of Claim 14 wherein the wide jumper strip has a C shaped configuration.

16. The semiconductor die stack of Claim 15 further comprising dielectric between the wide jumper strip and the interposed lead(s).

17. The semiconductor die stack of Claim 16 wherein the wide jumper strip is electrically connected to the middle portions of the leads.

18. The semiconductor die stack of Claim 17 wherein the wide jumper strip has a cross sectional area along its length equal to a cross sectional area along a height of the leads to which the wide jumper strip is attached.

19. The semiconductor die stack of Claim 18 wherein the wide jumper strip may be fabricated from the same material as the leads of the semiconductor die.

20. A method of vertically stacking a plurality of semiconductor dies, the stacking method comprising the steps of:

a) providing a semiconductor die with leads extending from side surfaces of the semiconductor die;

b) electrically connecting at least two leads of the semiconductor die;

c) stacking another semiconductor die on top of the semiconductor die so as to electrically connect leads of the upper semiconductor die to respective ones of the leads of the lower semiconductor die;

d) electrically connecting at least two leads of the top semiconductor die; and

e) repeating steps c) and d) at least once.

21. The method of Claim 20 wherein steps b) and d) of electrically connecting at least two leads of the semiconductor die are accomplished with narrow jumper strips.

22. The method of Claim 20 wherein steps b) and d) of electrically connecting at least two leads of the semiconductor die are accomplished with wide jumper strips.

23. The method of Claim 20 wherein steps b) and d) of electrically connecting at least two leads of the semiconductor die are accomplished with jumper plates.

24. The method of Claim 20 wherein steps b) and d) of electrically connecting at least two leads of the semiconductor die are accomplished with a guide(s).

25. The method of Claim 20 further comprising the step of maintaining a clamping force on the stacked semiconductor dies.

26. The method of Claim 20 wherein the stacking step c) comprises the steps of:

i) aligning second junctions of the leads of the upper semiconductor die with respective ones of the first junctions of the leads of the lower semiconductor die; and

ii) applying a clamping force on the stacked semiconductor dies.